Notice of Allowability	Application No.	Applicant(s)	
	10/604,097	DORIS ET AL.	
	Examiner	Art Unit	
	Pamela E. Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed on 1 December 2004*.

2. ☒ The allowed claim(s) is/are *1-11*.

3. ☒ The drawings filed on *08 August 2003* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

DETAILED ACTION

This office action is response the amendment filed on 1 December 2004. Claims 1-18 are pending.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

Please Claims 12-18.

Allowable Subject Matter

Claims 1-11 are allowed.

Reasons for Allowance

The following is an examiner's statement of reasons for allowance: prior art does not anticipate, teach, or suggest protecting the FET region and trimming the at least one patterned hard mask in the FinFET region, wherein each trimmed patterned hard mask in the FinFET region has a horizontal surface whose width is less than the width of that of each patterned hard mask in the FET region.

For example, Muller et al. (6,252,284) disclose a method of forming an integrated semiconductor circuit where a silicon-on-insulator structure comprises at least a top semiconductor layer located on a buried insulating layer, the top semiconductor layer having at least one patterned hard mask located in a FinFET region of the structure and at least one patterned hard mask located in a FET region of the structure; protecting the FET region and trimming the at least one patterned hard mask in the FinFET region, wherein the protecting the FET region comprising applying a resist mask to the FET region; etching exposed portions of the top semiconductor that are not protected with the hard masks stopping on the buried insulating layer, the etching defining a FinFET active device region and a FET active device region, the FinFET active device region being perpendicular to the FET active device region; forming a gate dielectric on each exposed vertical surface of the FinFET active device region, while forming a gate dielectric on an exposed horizontal surface of the FET device region; forming a patterned gate electrode on each exposed surface of the gate dielectric; and forming spacers abutting the patterned gate electrode.

Muller et al. further disclose the trimming including a chemical oxide removal process or a wet etch process. Muller et al. also disclose forming the patterned gate electrodes by depositing a gate conductor material; forming a patterned resist on top of the gate conductor material; and etching exposed portions of the gate conductor not protected with the patterned resist.

However, Muller et al. do not disclose, anticipate, teach, or suggest protecting the FET region and trimming the at least one patterned hard mask in the FinFET region,

wherein each trimmed patterned hard mask in the FinFET region has a horizontal surface whose width is less than the width of that of each patterned hard mask in the FET region; etching exposed portions of the top semiconductor that are not protected with the hard masks stopping on the buried insulating layer, the etching defining a FinFET active device region and a FET active device region, the FinFET active device region being perpendicular to the FET active device region; protecting the FinFET active device region and thinning the FET active device region so that the FET device region has a height that is less than the height of the FinFET active device region.

Ono (6,166,413) discloses a method of forming an integrated semiconductor circuit where a silicon structure comprises at least a top semiconductor layer, the top semiconductor layer having at least one patterned hard mask located in a first FET region of the structure and at least one patterned hard mask located in a second FET region of the structure; protecting the second FET region and trimming the at least one patterned hard mask in the first FET region, wherein the protecting the second FET region comprising applying a resist mask to the second FET region; protecting the first FET active device region and thinning the second FET active device region so that the second FET device region has a height that is less than the height of the first FET active device region, wherein the protecting the first FET active device region comprises applying a resist mask to the first FET active device region; etching exposed portions of the top semiconductor that are not protected with the hard masks, the etching defining a first FET active device region and a second FET active device region; forming a gate dielectric on an exposed horizontal surface of the first and second FET device regions;

forming a patterned gate electrode on each exposed surface of the gate dielectric; and forming spacers abutting the patterned gate electrode.

Ono further discloses the thinning including an etching process that is highly selective to SiO_2. Ono also discloses the patterned hard masks are formed by the steps of: forming an oxide layer on a surface of the top semiconductor layer; forming a mask layer on the oxide layer; applying a photoresist to an exposed surface of the mask layer; exposing the photoresist to a pattern of radiation; developing the pattern into the photoresist; and transferring the pattern from the photoresist into the mask layer and the oxide layer.

However, Ono does not disclose, anticipate, teach or suggest protecting the FET region and trimming the at least one patterned hard mask in the FinFET region, wherein each trimmed patterned hard mask in the FinFET region has a horizontal surface whose width is less than the width of that of each patterned hard mask in the FET region.

The prior art made of record in this action does not anticipate, teach, or suggest a method of forming an integrated semiconductor circuit where a silicon-on-insulator structure comprising at least a top semiconductor layer locating on a buried insulating layer, the top semiconductor layer having at least one patterned hard mask located in a FinFET region of the structure and at least one patterned hard mask located in a FET region of the structure; protecting the FET region and trimming the at least one patterned hard mask in the FinFET region, wherein each trimmed patterned hard mask in the FinFET region has a horizontal surface whose width is less than the width of that of each patterned hard mask in the FET region; etching exposed portions of the top

semiconductor that are not protected with the hard masks stopping on the buried insulating layer, the etching defining a FinFET active device region and a FET active device region, the FinFET active device region being perpendicular to the FET active device region; protecting the FinFET active device region and thinning the FET active device region so that the FET device region has a height that is less than the height of the FinFET active device region; forming a gate dielectric on each exposed vertical surface of the FinFET active device region, while forming a gate dielectric on an expose horizontal surface of the FET device region; and forming a patterned gate electrode on each exposed surface of the gate dielectric.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E. Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PEP

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800